

## METHOD OF FORMING MOS TRANSISTOR

This is a continuation-in-part of Application Serial No.: 10/455,600,  
5 entitled "METHOD OF FORMING MOS TRANSISTOR" filed June 5, 2003.  
The disclosure of which in its entirety is incorporated by reference herein.

### BACKGROUND OF THE INVENTION

10 1. Field of the Invention

The present invention relates generally to methods of forming  
MOS transistors, and more particularly to methods of simultaneously  
forming MOS transistors and a capacitor, an electrically erasable and  
programmable read only memory or a resistance on a substrate having  
15 gate insulation layers of varying thicknesses.

2. Discussion of Related Art

In a semiconductor integrated circuit (IC), electrical devices such as a transistor, a capacitor and a resistor are integrated into a chip.  
Therefore, methods for effectively integrating these electrical devices into a chip have been developed. For example, a method of simultaneously forming a plate electrode of a poly-insulation-poly (PIP) capacitor and a gate electrode of a MOS transistor is taught in US Patent no. 6,303,455, entitled "Method of fabricating capacitor".  
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There have been extensive studies on simultaneously employing logic technologies for processing data (e.g., CPU technologies) and memory technologies for storing data. In addition, transistor technologies have been adapted to the logic and memory technologies. The current supplying ability of a transistor, and its low leakage current  
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and high breakdown voltage characteristics are important in the memory technology. Therefore, a novel method to effectively embody MOS transistors having insulation layers of varying thicknesses in a single chip is needed.

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### **SUMMARY OF THE INVENTION**

An embodiment of the present invention provides a method of forming MOS transistors having insulation layers of varying thicknesses from each other.

10        According to another embodiment of the present invention, a method of forming a semiconductor device includes forming field regions in a substrate to define a first transistor region, a capacitor region, and a second transistor region. Simultaneously, a first gate stack is formed in the first transistor region and a lower electrode is formed in the capacitor region. Then, an upper electrode is formed on the lower electrode with a dielectric layer interposed therebetween and a second gate stack is simultaneously formed in the second transistor region.  
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20        According to another embodiment of the present invention, a method of fabricating a semiconductor device comprises forming field regions in a substrate to define a first transistor region, a capacitor region and a second transistor region. Simultaneously, a gate pattern is formed in the first transistor region and a lower electrode is formed in the capacitor region. Next, an upper electrode is formed on the lower electrode with a dielectric layer interposed therebetween and a second gate stack is simultaneously formed in the second transistor region. Then,  
25        the gate pattern is patterned to form a first gate stack, wherein forming the upper electrode with dielectric layer interposed thereunder and the second gate stack comprises forming a dielectric layer on the lower electrode, forming a second insulation layer and a second conductive

layer, and patterning the second conductive layer and the second insulation layer to form the upper electrode and the second gate stack.

According to another embodiment of the present invention, a method of forming a semiconductor substrate comprises: forming 5 isolation layers in predetermined regions of a semiconductor substrate to define a first region, a second region and a third region; forming a first gate insulating layer and a first gate conductive pattern stacked sequentially on the first region, a second gate insulating layer and a second gate conductive pattern stacked sequentially on the second region, 10 and a third gate insulating layer and the second gate conductive pattern stacked sequentially on the third region; and patterning together the first gate conductive pattern and the second gate conductive pattern to form a first gate electrode, a second gate electrode and a third gate electrode in the first, second and third regions, respectively. Further, the first gate insulating layer, the second gate insulating layer and the third insulating 15 layer have varying thicknesses and each layer has a different thickness as compared to the other layers.

Preferably, the step of forming isolation layers comprises forming the first gate insulating layer and the first gate conductive pattern stacked sequentially on the first region, forming the second gate insulating layer and the third insulating layer on the second region and the third region, respectively, wherein the thickness of the second gate insulating layer differs from the thickness of the third insulating layer. Next, a second gate conductive layer is formed on the entire surface of 20 the semiconductor substrate having the second and third gate insulating layers and the second gate conductive layer is patterned to form the second gate conductive pattern exposing the first gate conductive pattern in the first region. 25

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Figs. 1A-1D are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a first exemplary embodiment of the present invention.

5 Figs. 2A-2B are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a second exemplary embodiment of the present invention.

10 Figs. 3A-3E are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a third exemplary embodiment of the present invention.

Figs. 4A-4C are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a fourth exemplary embodiment of the present invention.

15 Figs. 5A-5E are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a fifth exemplary embodiment of the present invention.

20 Figs. 6A, 6B and 7 are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with the modifications of the fifth embodiment of the present invention.

## **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS**

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown.

25 A first transistor is formed in a region "A" and a capacitor is formed in a region "B." A second transistor is formed in a region "C." In any of exemplary embodiments discussed in relation to figures 1A-4C, the capacitor is formed in the region "B," but an electrically erasable and programmable read only memory (EEPROM) or a resistor may be formed

in region “B” as well. For example, a lower electrode of the capacitor corresponds to a floating gate of the EEPROM and a dielectric layer to inter-gate dielectric, an upper electrode of the capacitor to a control gate of the EEPROM. In addition, regions “A,” “B” and “C” of the drawings, referring to Figures 1A-4C, include two transistors, one capacitor and two transistors. This is for the convenience of explanation.

Figs. 1A-1D are cross-sectional views showing steps of forming MOS transistors in accordance with a first exemplary embodiment of the present invention.

Referring to Fig. 1A, field regions 4 are formed to define at least one active region in a substrate 2. In Fig. 1A, a predetermined region of the substrate 2 is selectively etched to form trenches. Then, the trenches are filled with an insulation material and polished using a chemical mechanical polishing to form the field regions 4. A first insulation layer and a first conductive layer are formed on a substrate including the field regions 4. A photolithographic process is performed to form a first gate stack 10 comprising a first gate insulation layer 6 and a first gate electrode 8 in region “A.” Simultaneously, a lower electrode 14 of a capacitor is formed in region “B.” The first gate insulation layer 6 is preferably formed of silicon oxide and the first conductive layer is preferably formed of polysilicon or any like material.

Referring to Fig. 1B, a dielectric layer 16 is formed on an entire surface of a substrate 2 including the first gate stack 10 and the lower electrode 14. The dielectric layer 16 is a material selected from the group consisting of silicon oxide, silicon nitride, oxide-nitride-oxide (ONO), tantalum oxide, barium-strontium-titanium (Ba-Sr-Ti) oxide, zirconium(Zr) oxide, hafnium (Hf) oxide, plumbum-zinc-titanium (Pb-Zn-Ti) oxide, strontium-bismuth-tantalum (Sr-Bi-Ta) oxide, and any combination thereof.

Referring to Fig. 1C, the dielectric layer 16 is patterned such that the dielectric layer 16 remains on the lower electrode 14 in region “B.”

Referring to Fig. 1D, a second insulation layer and a second conductive layer are sequentially stacked on an entire surface of the substrate 2. The second conductive layer and the second insulation layer are patterned by a photolithographic process to form a second gate stack 22 in region “C” and an upper electrode 26 of the capacitor in region “B.” The second gate stack 22 comprises a second gate insulation layer 18 and a second gate electrode 20. The second insulation layer 18 is formed having a different thickness than the first insulation layer 6, so that transistors in regions “A” and “C” may have different characteristics. In other words, a MOS transistor formed in region “C” can have different characteristics than a MOS transistor formed in region “A” and a capacitor formed in region “B.”

Source and drain regions are formed in the substrate on opposite sides of the gate stacks 10 and 22, respectively, to complete the formation of a MOS transistor (not shown).

Figs. 2A and 2B are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a second exemplary embodiment of the present invention.

Referring to Fig. 2A, field regions 4 are formed to define at least one active region in a substrate 2. A first insulation layer, a first conductive layer, and a dielectric layer are sequentially stacked on an entire surface of the substrate 2. The dielectric layer, the first conductive layer, and the first gate insulation layer are patterned by a photolithographic process to form a gate stack 19 in region “A.” Simultaneously, a lower electrode 14 and a dielectric layer 16 of a capacitor are formed in region “B.” The gate stack 19 comprises a first gate insulation layer 16, a first gate electrode 8, and a dielectric layer 16.

Referring to Fig. 2B, a second insulation layer and a second conductive layer are formed on an entire surface of the substrate. Then, the second insulating layer and the second conductive layer are patterned by a photolithographic process to form a second gate stack 22 in region “C” and an upper electrode 26 in region “B.” The second gate stack 22 comprises a second gate insulation layer 18 and a second gate electrode 20. The second insulation layer 18 is formed having a different thickness than the first gate insulation layer 6. In other words, transistors in region “A” and region “C” may have different characteristics from each other.

Source and drain regions are formed in a substrate on opposite sides of the gate stacks 19 and 22, respectively, thereby completing the formation of the MOS transistors.

In the second exemplary embodiment, the gate stack 19, the lower electrode 14, and the dielectric layer 16 are patterned at the same time, thereby reducing the number photolithographic steps for forming a semiconductor device.

Figs. 3A-3E are cross-sectional views showing steps of forming MOS transistors and a capacitor in accordance with a third exemplary embodiment.

Referring to Fig. 3A, field regions 4 are formed to define at least one active region in a substrate 2. A first insulation layer and a first conductive layer are sequentially formed on the substrate 2. The first conductive layer and the first insulation layer are patterned by a photolithographic process so as to form a gate pattern 11 in a region “A” and a lower electrode 14 in a region “B.” The gate pattern 11 comprises a first gate insulation layer 6 and a first gate conductive pattern 8. Preferably, edges of the gate pattern 11 overlap the field regions 4.

Referring to Fig. 3B, a dielectric layer 16 is formed on a substrate which includes the gate pattern 11 and the lower electrode 14.

Referring to Fig. 3C, the dielectric layer 16 is patterned by a photolithographic process such that the dielectric layer 16 remains on an entire surface of the gate pattern 11 in region “A” and the lower electrode 14 in region “B.”

5 Referring to Fig. 3D, a second insulation layer and a second conductive layer are sequentially stacked on an entire surface of the substrate. The second conductive layer and the second insulation layer are patterned by a photolithographic process to form a second gate stack 22 in a region “C” and an upper electrode 26 in region “B.” The second 10 gate stack 22 comprises a second gate insulation layer 18 and a second gate electrode 20. The second gate insulation layer 18 is formed having a different thickness than the first gate insulation layer 6.

Referring to Fig. 3E, the gate pattern 11 is patterned by a photolithographic process to form a first gate stack 19 in a region “A.”

15 Source and drain regions are formed in a substrate on opposite sides of the gate stacks 19 and 22, respectively, to complete the formation of a MOS transistor.

In the third embodiment, the dielectric layer 16 covers a top portion of the first gate stack 19 and serves as a barrier layer during a 20 subsequent ion implantation process. For example, while boron (B) ions are implanted to form a source and a drain of a PMOS, boron penetration is prevented by the dielectric layer 16.

Figs. 4A-4C are cross-sectional views showing steps of forming 25 MOS transistors and a capacitor in accordance with a fourth exemplary embodiment of the present invention.

Referring to Fig. 4A, field regions 4 defining at least one active region are formed in a substrate 2. Then, a first insulation layer, a first conductive layer, and a dielectric layer are sequentially stacked on an entire surface of a substrate 2. The dielectric layer, the first conductive

layer, and the first insulation layer are patterned by a photolithographic process to form a first gate pattern 17 in a region “A” and a lower electrode 14 and a dielectric layer 16 in a region “B.” The first gate pattern 17 comprises a first gate insulation layer 6, a first gate electrode 8 and a dielectric layer 16.

Referring to Fig. 4B, a second insulation layer and a second conductive layer are formed on an entire surface of the substrate. Then, the second conductive layer and the second insulation layer are patterned using a photolithographic process to form a second gate stack 22 in a region “C” and an upper electrode 26 in region “B.” The second gate stack 22 comprises a second gate insulation layer 18 and a second gate electrode 20. The second insulation layer 18 is formed having a different thickness than the first insulation layer 6.

Referring to Fig. 4C, the gate pattern 17 is patterned by a photolithographic process to form a first gate stack 19.

Source and drain regions (not shown) are formed in a substrate on opposite sides of the first and second gate stacks 19 and 22, respectively, to complete the formation of a MOS transistor.

In the fourth embodiment, the gate pattern 17, the lower electrode 14, and the dielectric layer 16 are simultaneously patterned, thereby reducing the number of photolithographic processes for forming semiconductor devices.

Figs. 5A to 5E are cross-sectional views illustrating a method of fabricating a semiconductor device in accordance with a fifth embodiment of the present invention.

Referring to Fig. 5A, isolation layers 4 are formed in a predetermined region of a semiconductor substrate 2 to divide the semiconductor substrate 2 into a plurality of regions. The regions may comprise a first region “A”, second region “B” and third region “C”. In

addition, the first region “A,” second region “B” and third region “C” may be classified by the operation voltages of transistors formed in their respective regions. According to this embodiment of the present invention, the first region “A”, second region “B” and third region “C” are active regions, which include transistors having operation voltages of 5.5V, 2.5V and 30V, respectively. Further, a part of the isolation layers 4 may be used to define a capacitor region “D” including a capacitor, as shown in Fig. 5A.

After forming the isolation layers 4, a first gate insulating layer 30 is formed on the first region “A.” The first gate insulating layer 30 may be a silicon dioxide layer, which is preferably grown to a thickness of between about 50 Å to about 300 Å by thermal oxidation. If the thermal oxidation process is applied to form the first gate insulating layer 30, the first gate insulating layer 30 may be formed on the entire surface of the semiconductor substrate 2. In this case, the first gate insulating layer 30 should be removed from the second region “B” and the third region “C,” and the removal of the first gate insulating layer 30 from the second region “B” and third region “C” can be accomplished by an additional process.

Next, a first gate conductive layer is formed on the semiconductor substrate 2 having the first gate insulating layer 30. According to another embodiment of the present invention, the first gate conductive layer may be a polycrystalline silicon layer having a thickness of between about 1000 Å to about 2000 Å. Alternatively, other conductive materials can be used for the first gate conductive layer. If the first gate conductive layer is formed of polycrystalline silicon, various doping methods such as in-situ doping, subsequent impurity diffusion and the like may be applied for doping the first gate conductive layer. Further, a desired impurity

concentration and desired conductivity of the first gate conductive layer can be obtained by controlling the doping process.

Next, the first gate conductive layer is patterned to form a first gate conductive pattern 62 in the first region "A" and a lower electrode 64 for a capacitor in the capacitor region "D." The patterning process of the first gate conductive layer may be utilized for the abovementioned removal of the first gate insulating layer 30 in the second region "B" and third region "C."

The first gate conductive pattern covers the entire surface of the first gate insulating layer 30. For covering the first gate insulating layer 30 entirely, the sidewalls of the first gate conductive pattern 62 are preferably placed on the isolation layers 4 in the first region "A." And, the lower electrode 64 of the capacitor is disposed on the isolation layer 4 in the capacitor region "D."

Referring to Fig. 5B, a dielectric layer is formed on the semiconductor substrate 2 having the first gate conductive pattern 62 and the lower electrode 64. The dielectric layer is then patterned to form a dielectric pattern 75 to cover the upper and side surfaces of the first gate conductive pattern 62 and the lower electrode 64. In addition, the dielectric layer is removed from the second region "B" and third region "C."

The dielectric layer is a material selected from the group consisting of silicon oxide, silicon nitride, oxide-nitride-oxide, tantalum oxide, barium-strontium-titanium oxide, zirconium oxide, hafnium oxide, plumbum-zinc-titanium oxide, strontium-bismuth-tantalum oxide, and any combination thereof. According to this embodiment of the present invention, the dielectric layer is preferably formed of an oxide-nitride-oxide layer.

Referring to Fig. 5C, after patterning the dielectric layer, a second gate insulating layer 40 and a third gate insulating layer 50 is formed on the second region “B” and the third region “C,” respectively. According to this embodiment of the present invention, the second gate insulating layer 40 may be a silicon dioxide layer, which is grown to a thickness of between about 10 Å to about 100 Å by thermal oxidation. And, the third gate insulating layer 50 is a silicon dioxide layer, which is deposited to a thickness of between about 100 Å to about 1000 Å by a chemical vapor deposition.

Further, the processes of forming the second insulating layer 40 and the third gate insulating layer 50 can comprise forming a first silicon oxide layer and a mask layer stacked sequentially on the second region “B” and third region “C.” Then, the mask layer is patterned to form a mask pattern that covers the second region “B” and exposes the third region “C.” Next, a second silicon oxide layer, which will be used as the third gate insulating layer 50, is formed on the semiconductor substrate 2 with the mask pattern using a chemical vapor deposition. The second silicon oxide layer, the mask pattern and the first silicon oxide layer are then patterned to expose the semiconductor substrate 2 in the second region “B.” Next, another silicon oxide layer, which will be used as the second gate insulating layer 40, is formed on the exposed semiconductor substrate 2 in the second region “B” by thermal oxidation.

In addition, a dielectric layer consisting of an oxide-nitride-oxide layer can replace the first silicon oxide layer, the mask layer and the second silicon oxide layer. Further, other processes can be envisioned based upon the method described above for forming the second and third gate insulating layers 40 and 50.

Referring to Fig. 5D, a second gate conductive layer is formed on the semiconductor substrate 2 having the second insulating layer 40 and the third gate insulating layer 50. Next, the second gate conductive layer is patterned to form a second gate conductive pattern 80 exposing the first region “A.” According to this embodiment of the present invention, the second gate conductive pattern 80 is removed from the first region “A” to expose the top surface of the dielectric pattern 75 thereof.

The second gate conductive pattern 80 is preferably formed of the same material as the first gate conductive pattern 62. According to this embodiment of the present invention, the first gate conductive pattern 62 and second gate conductive pattern 80 are preferably formed of a polycrystalline silicon layer.

Referring to Fig. 5E, the first gate conductive pattern 62 and the second gate conductive pattern 80 are patterned together to form first gate stacks 91, second gate stacks 92, a third gate stack 93 and a capacitor structure 95. The first gate stacks 91, second gate stacks 92, third gate stack 93 and capacitor structure 95 are formed on the first region “A,” second region “B,” third region “C,” and capacitor region “D,” respectively. Preferably, the patterning process is performed so that the semiconductor substrate 2 is exposed in the first region “A,” second region “B,” and third region “C,” and the dielectric pattern 75 is exposed in the capacitor region “D.”

Thus, the first gate stacks 91 comprise a first gate insulating pattern 30’, a first gate electrode 62’ and a first capping pattern 75’ sequentially stacked on the first region “A.” The second gate stacks 92 comprise a second gate insulating pattern 40’ and a second gate electrode 82 sequentially stacked on the second region “B,” and the third gate stack 93 comprises a third gate insulating pattern 50’ and a third gate electrode 84 sequentially stacked on the third region “C.” And, the

capacitor structure 95 comprises the capacitor lower electrode 64, the dielectric pattern 75 and the capacitor upper electrode 86 stacked sequentially on the isolation layer 4 in the capacitor region “D.” The capping pattern 75’ corresponds to the dielectric pattern 75 remaining on the first gate conductive pattern 62 after the above patterning.

The aforementioned fifth embodiment of the present invention can be modified as shown in Figs. 6A, 6B and 7. Further, the steps illustrated by Figs. 5A-5C are the same and will be omitted in the following explanation pertaining to the following modifications of the fifth embodiment.

Referring to Figs. 5C and 6A, an anti-reflecting layer 90 is formed on the second gate conductive layer before patterning the second gate conductive layer, and then a photo resist pattern (not shown) exposing the first region “A” is formed on the anti-reflecting layer 90. Next, the anti-reflecting layer 90 and the second gate conductive layer are sequentially patterned using the photo resist pattern as an etching mask. Thus, the second gate conductive pattern 80 and the anti-reflecting layer 90 stacked sequentially are formed on the second region “B”, third region “C”, and capacitor region “D” while exposing the dielectric pattern 75 on the first region “A.”

Referring to Fig. 6B, as shown in Fig. 5E, first gate stacks 91, second gate stacks 92, a third gate stack 93 and a capacitor structure 95 are formed on the first region “A,” second region “B,” third region “C” and capacitor region “D,” respectively. According to this modification of the fifth embodiment, the second gate stacks 92, the third gate stack 93 and the capacitor structure 95 comprise an additional anti-reflecting pattern 90’.

Preferably, the anti-reflecting layer is formed of a material that has a non-selective etching characteristic with respect to the dielectric

pattern 75 during the patterning process. For example, the anti-reflecting layer may be a material having an etching selectivity of between about 50 to about 150% with respect to the dielectric pattern 75 during the patterning process. To obtain this characteristic of an etching selectivity, 5 the anti-reflecting material is carefully selected and the thickness of the anti-reflecting material is controlled. Preferably, the anti-reflecting layer 90 is a material selected from a group consisting of a silicon oxide layer, a silicon oxynitride, a silicon nitride, and any combination thereof.

According to the fifth embodiment of the present invention, the 10 capacitor upper electrode 86 and the second gate conductive pattern 84 may be formed simultaneously. And, as shown in Figs. 6A and 6B, the anti-reflecting layer 90 is further formed on the second gate conductive layer before patterning the second gate conductive layer. During the patterning step shown in Fig. 6B, the capacitor region “D” may be 15 covered by a masking layer such as a photo resist pattern.

According to the fifth embodiment and modified embodiments thereof, three different gate stacks 91, 92 and 93 and a capacitor structure 95 are formed by performing a single gate patterning process, wherein the three different gate stacks 91, 92 and 93 have gate insulating 20 layers 30', 40' and 50', respectively. Further, the gate insulating layers 30', 40', and 50' can have different thicknesses.

In general, since the gate patterning process requires precise and strict control of process conditions, the fifth embodiment and its modifications comprising the single gate patterning process further 25 reduce the number of processes for forming a semiconductor device. Thus, the reduced number of processes can lower production cost as compared to the preceding embodiments. According to the fifth embodiment and its modified embodiments, the profile after etching

process can be minimized and improved. And, the abovementioned residue problem can be also prevented.

According to the embodiments of the present invention, MOS transistors including gate insulation layers having different thicknesses are formed using typical fabrication steps and structures of a capacitor, a resistance, an electrically erasable and programmable read only memory or the like.

While the present invention has been described in connection with specific and exemplary embodiments thereof, it is capable of various changes and modifications without departing from the spirit and scope of the invention.